than that of the lower surface metal foil;

forming an opening in the upper surface metal foil at a location corresponding to a blind via hole formation portion of the insulative substrate;

forming a blind via hole, the bottom of which is the lower surface metal foil, by emitting a laser against the blind via hole formation portion through the opening;

app1ying a conductor to the blind via hole; and

forming an upper surface pattern and a lower surface pattern by respectively etching the upper surface metal foil and the lower surface metal foil, wherein the upper surface and lower surface metal foil coating step includes a step of coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for etching the upper surface metal foil.

cont'd C1

5. (Amended) A method for manufacturing a printed circuit board comprising the steps of:

coating a lower surface and an upper surface of an insulative substrate respectively with a lower surface metal foil and an upper surface metal toil, the thickness of which is less than that of the lower surface metal foil;

forming an opening in the upper surface metal foil at a location corresponding to a blind via hole formation portion of the insulative substrate;

forming a blind via hole, the bottom of which is the lower surface metal foil, by emitting a laser against the blind via hole formation portion through the opening;

applying a conductor to the blind via hole; and

forming an upper surface pattern and a lower surface pattern by respectively etching the upper surface metal foil and the lower surface metal foil, wherein the upper surface and lower surface metal foil coating step includes a step for coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for performing a sandblast treatment to the upper surface metal foil so that the thickness of the upper surface metal foil becomes less that of

the lower surface metal foil.

6. (Twice Amended) The printed circuit board manufacturing method according to claim 3, wherein the thickness of the upper surface pattern is 2 to 12μm.

Cont'd C1

7. (Twice Amended) The printed circuit board manufacturing method according to claim 3, wherein the thickness of the lower surface pattern is 15 to 25μm.

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9. (Once Amended) A method for manufacturing a printed circuit board comprising the steps of:

coating a lower surface and an upper surface of an insulative substrate respectively with a lower surface metal, foil and an upper surface metal foil, the thickness of which is less than that of the lower surface metal foil;

C2

forming an upper surface pattern and a lower surface pattern by respectively etching the upper surface metal foil and the lower surface metal foil, wherein the upper surface pattern has an opening exposing the upper surface of the insulative substrate at a location corresponding to a blind via hole formation portion, and the lower surface pattern covers the lower surface of the insulative substrate at a location corresponding to the blind via hole formation portion;

forming a blind via hole, the bottom of which is the lower surface pattern, by emitting a laser against the, insulative substrate through the opening; and

applying a conductor to the blind via hole, wherein the upper surface end lower surface metal foil coating step includes a step of coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for etching the upper surface metal foil.

11. (Once Amended) A method for manufacturing a printed circuit board comprising the steps of:

coating a lower surface and an upper surface of an insulative substrate respectively with a lower surface metal, foil and, an upper surface metal foil, the thickness of which is less than that of the lower surface metal foil;

forming an upper surface pattern and a lower surface pattern by respectively etching the upper surface metal foil and the lower surface metal foil, wherein the upper surface pattern has an opening exposing the upper surface of the insulative substrate at a location corresponding to a blind via hole formation portion, and the lower surface pattern covers the lower surface of the insulative substrate at a location corresponding to the blind via hole formation portion;

forming a blind via hole, the bottom of which is the lower surface pattern, by emitting a laser against the insulative substrate through the opening; and

cont'd C2

applying a conductor to the blind via hole, wherein the upper surface and lower surface metal foil coating step includes a step for coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for performing a sandblast treatment to the upper surface metal foil so that the thickness of the upper surface metal foil becomes less that of the lower surface metal foil.

12. (Once Amended) The printed circuit board manufacturing method according to claim 9, wherein the thickness of the upper surface pattern is 2 to 12μm.

13. (Once Amended) The printed circuit board manufacturing method according to claim 9, wherein the thickness of the lower surface pattern is 15 to 25μm.

Please add claims 14-17, as follows:

C3

14. The printed Circuit board manufacturing method according to claim 5, wherein the thickness of the upper surface pattern is 2 to 12μm.

15. The printed Circuit board manufacturing method according to claim 5, wherein the thickness of the lower surface pattern is 15 to 25μm.

Canted C3

16. The printed circuit board manufacturing method according to claim 11, wherein the thickness of the upper surface pattern is 2 to 12μm.

17. The printed circuit board manufacturing method according to claim 11, wherein the thickness of the lower surface pattern is 15 to 25μm.

REMARKS

In the Official Action (second) mailed on July 5, 2002, the Examiner rejected claims 1, 2, 4 and 10 under 34 U.S.C. § 102 (e) as being anticipated by U.S. Patent 6,346,687 granted to Kono et al., rejected claim 8 under § 102(b) as being anticipated by U.S. Patent 4,694,212 granted to Deroux-Dauphin et al., and rejected claims 6, 7, 12 and 13 under § 103(a) as being obvious in view of Kono (the U.S. '678 patent). However, the Examiner also said that dependent claims 3, 5, 9 and 11 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

In response, claims 1, 2, 4 and 10 have been canceled and claims 3, 5, 9 and 11 have been amended in independent form. New claims 14 and 16, which are similar to claim 6, have been added, and new claims 15 and 17, which are similar to claim 7, have been added. By the foregoing amendment, claims 3, 5, 7 and 11 and their dependent claims 6, 7 and 12-17 are pending and believed to be in condition for allowance.

Concerning the rejection of claim 8, the Examiner states that Deroux-Dauphin et al. discloses an upper surface pattern (32) the thickness of which is less than that of a lower surface pattern (36). Although it may appear to look that way in Fig. 7, the size of the lower surface pattern (36) and the upper surface pattern (32) is not specifically described in the specification of Deroux-Dauphin patent. To the contrary, the specification states that "the